Pranav Gangwar

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Summary

Interested in pursuing a research career in Domain Specific Accelerators especially for Machine Learning, Hyperdimensional Computing, and Homomorphic Encryption.

Education

- **University of California, San Diego** — San Diego, US
  PhD in Computer Engineering; GPA: 4.0/4.0 — *Sep. 2021*
  Coursework : Computer Architecture (CSE 240A), VLSI for Machine Learning (ECE 284), Operating Systems (CSE 120), Hyperdimensional Computing(CSE 291)

- **Delhi Technological University** — Delhi, India
  BTech in Electronics and Communication; Aggregate: 83.33% — *Aug. 2014 – Jun 2018*

Publications

- **Hardware/Software Co-Design of a High-Speed Othello Solver** — Dallas, USA
  IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS) — *August 2019*
- **Novel Control Unit Design for a High-Speed SHA-3 Architecture** — Dallas, USA
  IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS) — *August 2019*

Research Projects

- **Bit Serial CNN Accelerator** — SEE Lab
  - Proposed an architecture that takes advantage of the novel bit skipping concept
  - Ensured maximal reuse of the data stored on chip
- **Homomorphic Encryption Accelerator** — SEE Lab
  - Designing a complete end-to-end system working on Homomorphic Encryption scheme

Academic Projects

- **Systolic Array Implementation for VGGNet** — UCSD
  in partial fulfillment of the course ECE 284 - Low Power VLSI for Machine Learning — *Fall 2021*
  - Designed a 2-D Systolic Array and its auxiliary interfaces to perform convolutions in weight stationary fashion
  - Fetched only effectual input activations from SRAM corresponding to the loaded weights
  - Parallelized and overlapped the partial sum addition with the Processing Element working
  - Code written in System Verilog, tested with golden vectors generated in PyTorch and synthesized on Quartus

- **Dynamic Branch Predictor** — UCSD
  in partial fulfillment of the course CSE 240A - Principles of Computer Architecture — *Fall 2021*
  - Implemented Gshare & Tournament predictors with Branch Target Buffer(BTB) and analyzed misprediction rates
  - Designed a Hierarchical Branch Predictor that produced lower misprediction rate compared to above ones

Professional Experience

- **Texas Instruments** — Bangalore, India
  Digital Design Engineer — *July 2018 - July 2021*
  - Designed entire back-end of blocks: Floorplan, Placement, Clock Tree Synthesis, and Routing
  - Performed Timing and Physical Verification sign-off checks
  - Helped restructure pipeline of blocks to meet stringent input-output timing constraints
  - Created an area-efficient Transpose filter script that generated designs with lower area than hand-coded RTL
  - Developed Total Power Recovery flow which reduced power by taking advantage of lower pessimism of Sign-off than P&R

Technical Skills

- **Languages**: C, Verilog, Python, Tcl, Shell
- **Softwares**: PyTorch, Innovus™, Tempus™, Voltus™, PVS, Assura®, Vivado ®, MATLAB ®, PSpice